REMARKS/ARGUMENTS

The above-identified patent application has been reviewed in light of the Examiner's Action mailed 13 March 2003 (Paper No. 7). Claims 1-23 were pending. Claims 7 and 11-14 have been amended herein. Claims 15-17 and 20-23 have been cancelled without intending to abandon or to dedicate to the public any patentable subject matter. Accordingly, following entry of the foregoing amendments, Claims 1-14, 18 and 19 will be pending. As set forth more fully below, reconsideration and withdrawal of the Examiner's rejections of the claims are respectfully requested.

Objection to the Claims

The Examiner has objected to Claim 7 having the recitation "andor" in line 2. Applicants have amended Claim 7 to recite "and."

Rejections Under 35 U.S.C. § 112, Second Paragraph

The Examiner has rejected Claims 11-14 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Specifically, the Examiner notes that there is insufficient antecedent basis for the recitation of "the polishing process" in line 1 of these claims. Applicants have amended these claims to recite "the method for preparing multicrystalline substrates."

Applicants therefore submit that Claims 11-14, as amended are sufficiently definite to meet the requirements of 35 U.S.C. § 112, second paragraph.

Claim Rejections Under 35 U.S.C. § 103

The Examiner has rejected Claims 1-3 and 5-8 under 35 U.S.C. § 103(a) as obvious over U.S. Patent No.6,328,796 (Kub) in view of U.S. Patent No. 6,057,212 (Chan). The Examiner cites Kub as teaching all limitations of the rejected claims except processing to a surface roughness of below 20 Angstroms. The Examiner cites Chan as showing a surface roughness of less than 5 Angstroms. The Examiner argues that because both Chan and Kub are from the same

field of endeavor, it would have been obvious to use the method of Kub to obtain the surface roughness specified in Cub. Applicants respectfully disagree for the following reasons.

The focus of Kub is to epitaxially grow single crystalline layer(s) on high quality and expensive poly-crystalline ceramic substrates, primarily 3C-SiC. These substrates are quite different from the multi-crystalline "low-cost" silicon of the present invention. Kub does not teach or suggest that the disclosed method of processing substrates having a microscopic structure of a ceramic poly-SiC substrate would function in preparing a multi-crystalline silicon substrate of the present invention, nor is it obvious that a similar approach would work.

Additionally, Kub first bonds a single crystalline seed material to the poly-crystalline ceramic substrate that is optionally coated with a filler layer. In section 4, line 14 Kub discloses that this filler layer can be polished to less than 1nm for bonding, but Kub does not teach how this is done. Because Kub does not teach how to polish this filler material, the Examiner's assertion that Kub teaches polishing the surface of the filler layer to form a substantially smooth upper surface on the substrate is incorrect.

Chan provides a method of making an inert, conductive layer underneath a silicon oxide layer. Chan makes no reference to using a CVD poly-silicon layer as bonding layer. Chan does disclose that a smooth layer needs to be formed prior to bonding (which is a trivial statement) but does not teach how this is done. The disclosure of Chan referring to "touch polishing" to achieve 0.5nm roughness, is in reference to a single crystalline material (i.e. the surface of an SOI wafer) prior to bonding, not to polishing of poly- or multi-crystalline silicon or a filler layer. Thus, neither Kub nor Chan teaches the polishing of poly-crystalline silicon material as claimed in the present invention.

Both Chan and Kub specify a surface roughness of 0.2 – 2 nm which is just a common requirement for bonding. The exceptional advantage of the present invention is achieving this smoothness on each particular material thereby allowing the bonding and use of less expensive materials than were previously required. Therefore, Applicants submit that the combination of

Kub and Chan does not teach every limitation of the present invention and that there is no suggestion or motivation in the two patent references to make the presently-claimed invention and respectfully request that this rejection under 35 U.S.C. § 103(a) be withdrawn.

The Examiner has rejected Claims 1, 7-8 and 10 under 35 U.S.C. § 103(a) as obvious over U.S. Patent No.6,500,694 (Enquist) in view of Kub. The Examiner cites Enquist as teaching all limitations of the rejected claims except an initial substrate composed of a multi-crystalline substrate. The Examiner cites Kub as employing a multi-crystalline substrate. The Examiner then argues that it would have been obvious to use the process of Enquist on the starting material of Kub.

The focus of Enquist is the integration of three-dimensional devices by bonding to certain substrates. Enquist teaches adding a bonding layer to an already structured wafer, which is then planarized to achieve 0.5nm smoothness for bonding. However, according to the disclosure of Enquist, this bonding layer consists of silicon oxides, not the polysilicon of the present invention. While Enquist discloses that the substrate for bonding may be engineered to provide additional functionality to the bonded semiconductor device like improved transfer of heat, electrical interconnects, antennae, Enquist does not teach or suggest the concept of a low cost multi-crystalline material as a substrate. On the other hand, Kub uses poly-crystalline substrates only in the context of ceramic materials (SiC, diamond, graphite, AlN) for improved heat transfer and compliance with non-silicon semiconductors. Thus, neither reference teaches or suggests the use of a multicrystalline substrate in the process of the present invention nor is there any reasonable expectation of success that one of skill in the art could use the ceramic materials of Kub in the process of Enquist to form a ceramic bonding layer to bond to three dimensional devices.
For this reason, Applicants submit that the combination of Enquist and Kub does not teach every limitation of the present invention and that there is no reasonable expectation of success that the two patent references could be combined to make the presently claimed invention and respectfully request that this rejection under 35 U.S.C. § 103(a) be withdrawn.

The Examiner has rejected Claims 4, 6 and 9 under 35 U.S.C. § 103(a) as obvious over Enquist and Kub and further in view of Statutory Invention Registration No. H1137 (Easter). The Examiner cites the teachings of Enquist and Kub as noted above and Easter for the use of a polycrystalline silicion formed by low prossure CVD.

Applicants note that the combination of Enquist and Kub does not teach the presently claimed method for the reasons described above. Further, Applicants submit that Easter discloses the growth of a LPCVD poly-silicon layer as a bonding interface to create a replacement for DI wafers. However, this layer is grown on a single crystalline, structured substrate – not a multi-crystalline silicon wafer. Applicants note that the microscopic structure as well as the physical and chemical properties of multi-crystalline silicon are quite different from single crystalline silicon and therefore a modification of either Enquist or Kub using Easter as a guideline would not produce the presently claimed method and one of skill in the art would not have a reasonable expectation of success of combining the teachings of these references to form any functional wafer processing method. Therefore, Applicants submit that the combination of Enquist, Kub and Easter does not teach every limitation of the present invention and that there is no reasonable expectation of success for combining these three patent references into a functional wafer preparation process and respectfully request that this rejection under 35 U.S.C. § 103(a) be withdrawn.

The Examiner has rejected Claim 18 under 35 U.S.C. § 103(a) as obvious over U.S. Patent No. 5,571,373 (Krishna) in view of Chan. The Examiner cites Krishna as teaching a rough polishing step using an alkaline slurry while changing the composition of the slurry by feeding neutral polishing slurry to the polishing pad while reducing the supply of the rough polishing slurry. The Examiner cites Chan as teaching polishing to a surface roughness of less than 0.5 nm. The Examiner then argues that Krishna and Chan are in the same field of endeavor and therefore, it would have been obvious to use the method of Krishna to achieve a surface roughness of less than 0.5 nm.

Applicants submit that Krishna and Chan refer to polishing of single crystalline silicon. The process described by Krishna would not be applicable to multi-crystalline silicon because of etching of grain boundaries during the first polishing step. Also, Applicants are unclear as to the reference in Krishna to feeding a neutral polishing slurry. In fact, Krishna describes in great detail the change of a sodium stabilized slurry to an ammonia stabilized colloidal slurry to improve the surface roughness on single crystalline wafers. This recipe would not work with multi-crystalline wafers because both slurries are very alkaline (pH 9 – 11). In the presently claimed process, the first slurry is only weakly alkaline (pH 7 – 9) and the second slurry is neutral (pH 7). It is not obvious that recipes that work well for single crystalline material can be applied to multi- or poly-crystalline silicon. Indeed, the modifications to achieve smooth surfaces on multi- or poly-crystalline Si are not trivial and are not taught nor rendered obvious by the disclosure of Krishna or the combination Krishna and Chan. Therefore, Applicants submit that the combination of Krishna and Chan does not teach every limitation of the present invention and that there is no reasonable expectation of success for this combination and respectfully request that this rejection under 35 U.S.C. § 103(a) be withdrawn.

The Examiner has rejected Claim 19 under 35 U.S.C. § 103(a) as obvious over Krishna and Chan in view of U.S. Patent No. 5,821,167 (Fukami). The Examiner cites Krishna and Chan as described above and Fukami for the double-sided polishing of a semiconductor wafer. The Examiner argues that it would have been obvious to combine the teaching of Fukami with Krishna and Chan to produce the process of the instant Claim 19.

Applicants submit that Fukami does not overcome the problems of the combination of Krishna and Chan noted above. Further, Fukami teaches double side polishing primarily to find a combination of steps that achieve a low brightness backside with a high brightness front side to emulate conventional, single-sided polished wafers. All examples provided in Fukami refer to single crystalline CZ grown silicon wafers. Nowhere does Fukami disclose polishing of multi- or poly-crystalline silicon. As noted above with respect to Krishna, the polishing compounds of

Fukami and Krishna would not work with a poly-crystalline material. Applicants submit that the combination of Krishna, Chan and Fukami does not overcome the problems noted with respect to Claim 18 above and that there is no reasonable expectation of success for this combination and therefore, respectfully request that this rejection under 35 U.S.C. § 103(a) be withdrawn.

In light of these comments, Applicants submit that all pending claims are in condition for allowance and such disposition is respectfully requested. In the event that a telephone conversation would further prosecution and/or expedite allowance, the Examiner is invited to contact the undersigned.

Respectfully submitted,

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Attachments